ZZZ4 LS-4764P

PCB

DA80000CG00

Compal Confidential

KIU10 LS-4764P
Schematics Document

Menlow-Silverthorne with Poulsbo

REV:1.0
2008/12/02

Security Classification	Compal Secret Data		
Issued Date	2008/07/15	Deciphered Date	2011/07/15

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Title: *Cover Sheet*

Size: Custom | Document Number: *KIU10 LS-4764P* | Rev: 1.0

Date: | Sheet 1 of 20

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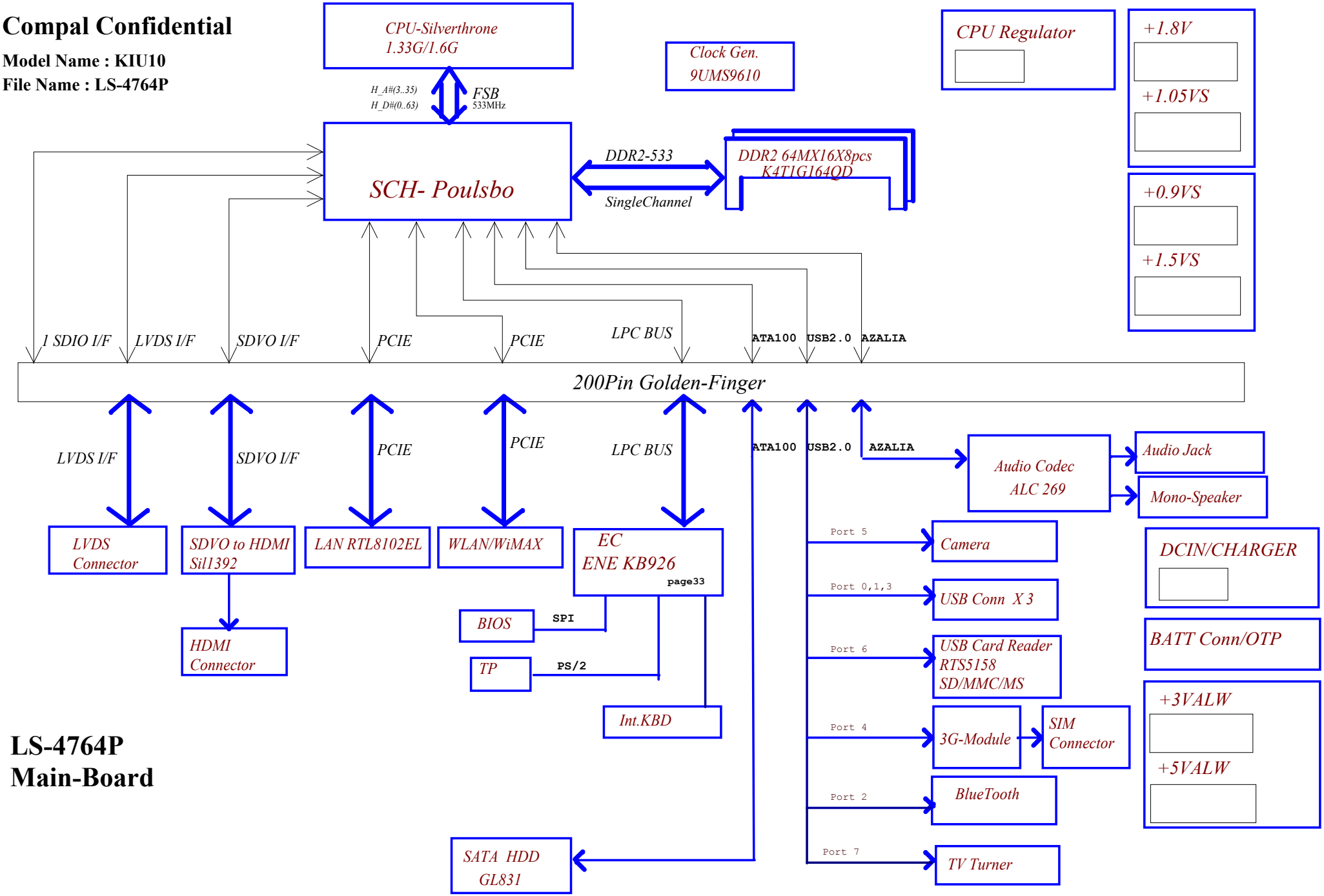
Model Name : KIU10
File Name : LS-4764P



LS-4764P
Main-Board

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Title: **Block Diagram**

Size	Document Number	Rev
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Date: Tuesday, December 02, 2008 | Sheet 2 of 20

Voltage Rails

O MEANS ON X MEANS OFF

State \ power plane	+VBAT	+5VALW +3VALW	+1.8V +0.9V	+5VS +3VS +1.8VS +1.5VS +CPU_CORE +VCCP	CLOCK
S0	O	O	O	O	O
S3	O	O	O	X	X
S5 S4/AC	O	O	X	X	X
S5 S4/ Battery only	O	X	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X	X

O MEANS ON
X MEANS OFF

S3 : STR
S4 : STD
S5 : SOFT OFF

SKU ID Table

Vcc	3.3V +/- 5%
Ra	100K +/- 5%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
* 0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

SKU ID	MB ID(H)	MB ID(L)
0		
* 1	IEL10	
2	IDL11	IDL01
3	HDL10	HDL00
4		HDL20
5	IDL12	HDL30
6		
7		

	MB ID
H	15"
L	14"

TBD

BOM Structure

MARK	FUNCTION
@	NC FOR ALL

Address

USB PORT LIST

PORT	DEVICE
0	2A POWER USB
1	USB (right)
2	BT
3	USB(lEFT)
4	3G, GPS
5	Camera
6	Card reader
7	TV Turner

EC SM Bus1 address

Device	Address
EEPROM(24C16/02)	1010 000X b

EC SM Bus2 address

Device	Address
ADM1032	1001 100X b

Poulsbo SM Bus address

Device	Address
Clock Generator (ICS954226)	1101 001Xb

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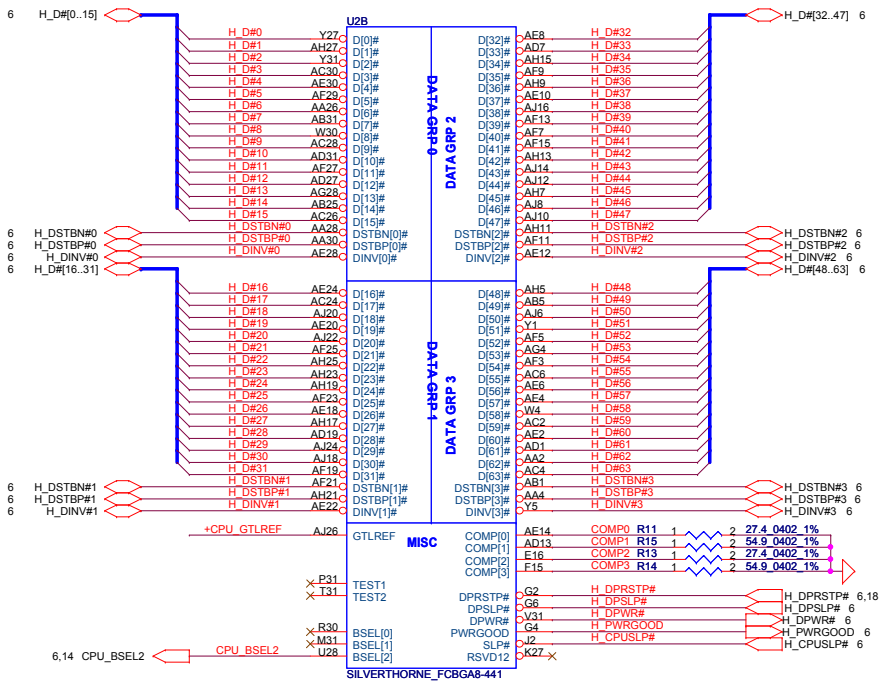
Silverthrone Host Data Interface

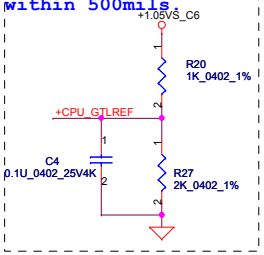


layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

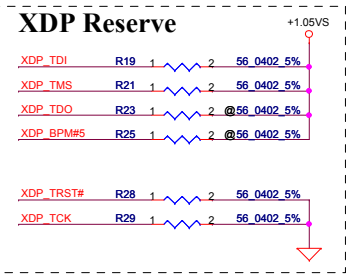
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
100	1	0	1
133	0	0	1

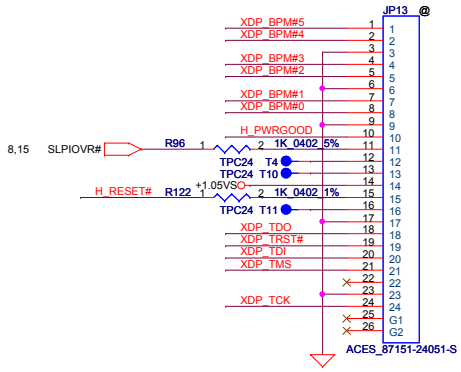
Resistor placed within 0.5" of CPU pin.Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

Close to CPU pin AD26 within 500mils

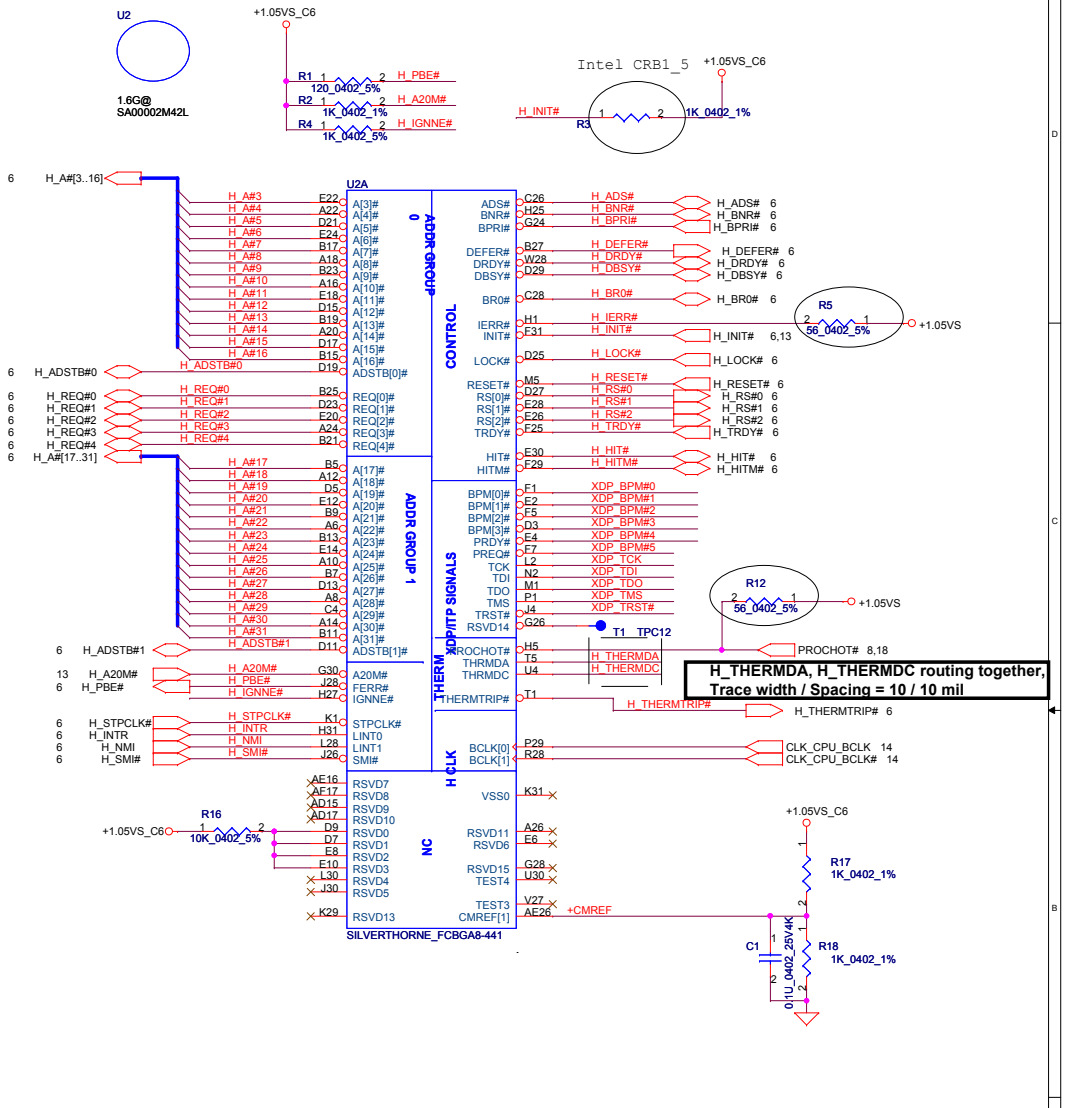


XDP Reserve



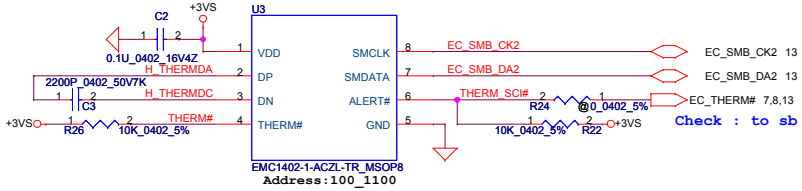


Silverthrone Host Data Interface



H_THERMDA, H_THERMDC routing together, Trace width / Spacing = 10 / 10 mil

Thermal Sensor



Check : to sb

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Compal Electronics, Inc.

Title: Silverthorne(1/2)-AGTL+/XDP

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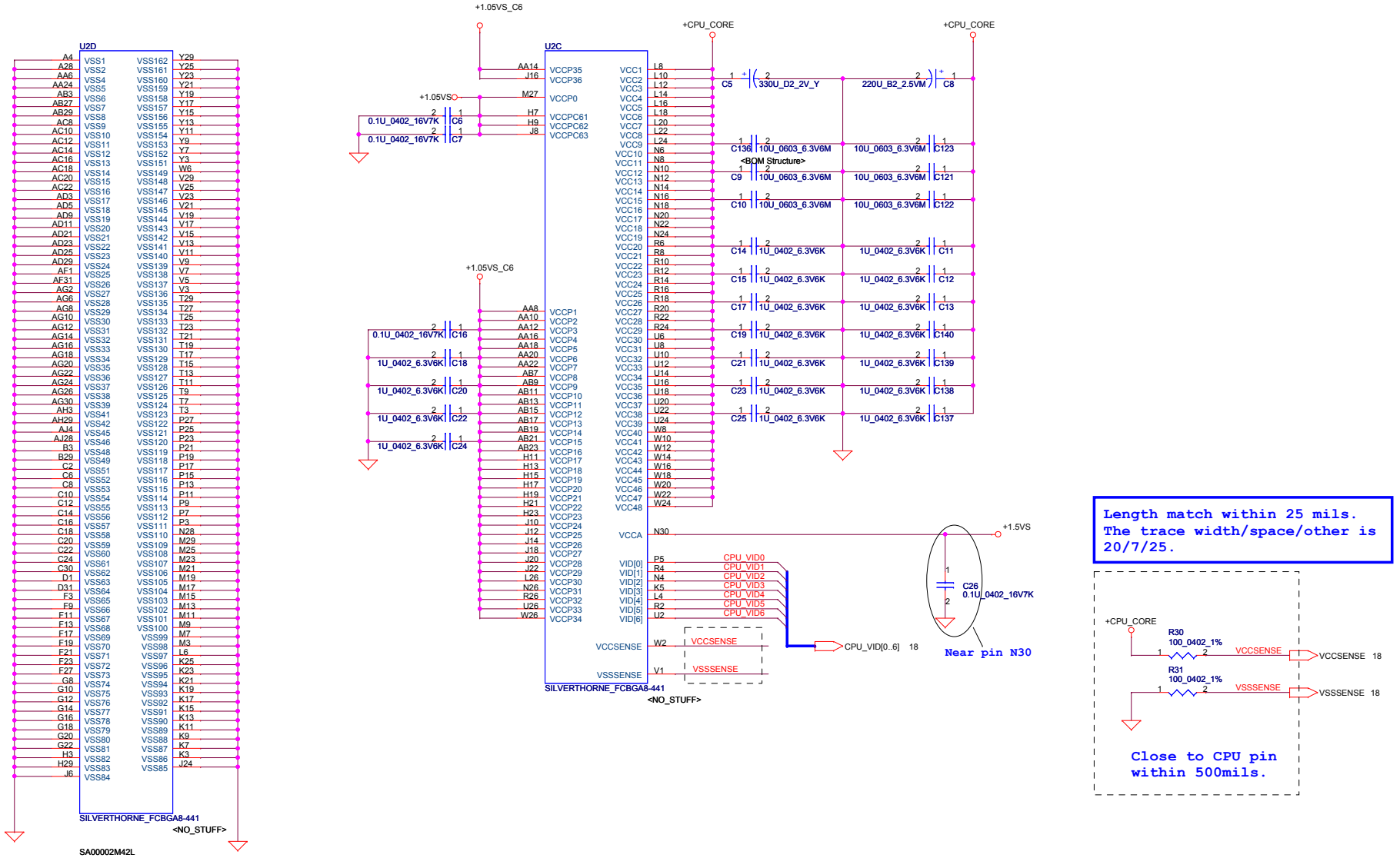
Date: Tuesday, December 02, 2008 | Sheet 4 of 20



Length match within 25 mils.
The trace width/space/other is 20/7/25.

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Title: Silverthorne(2/2)-PWR/GND

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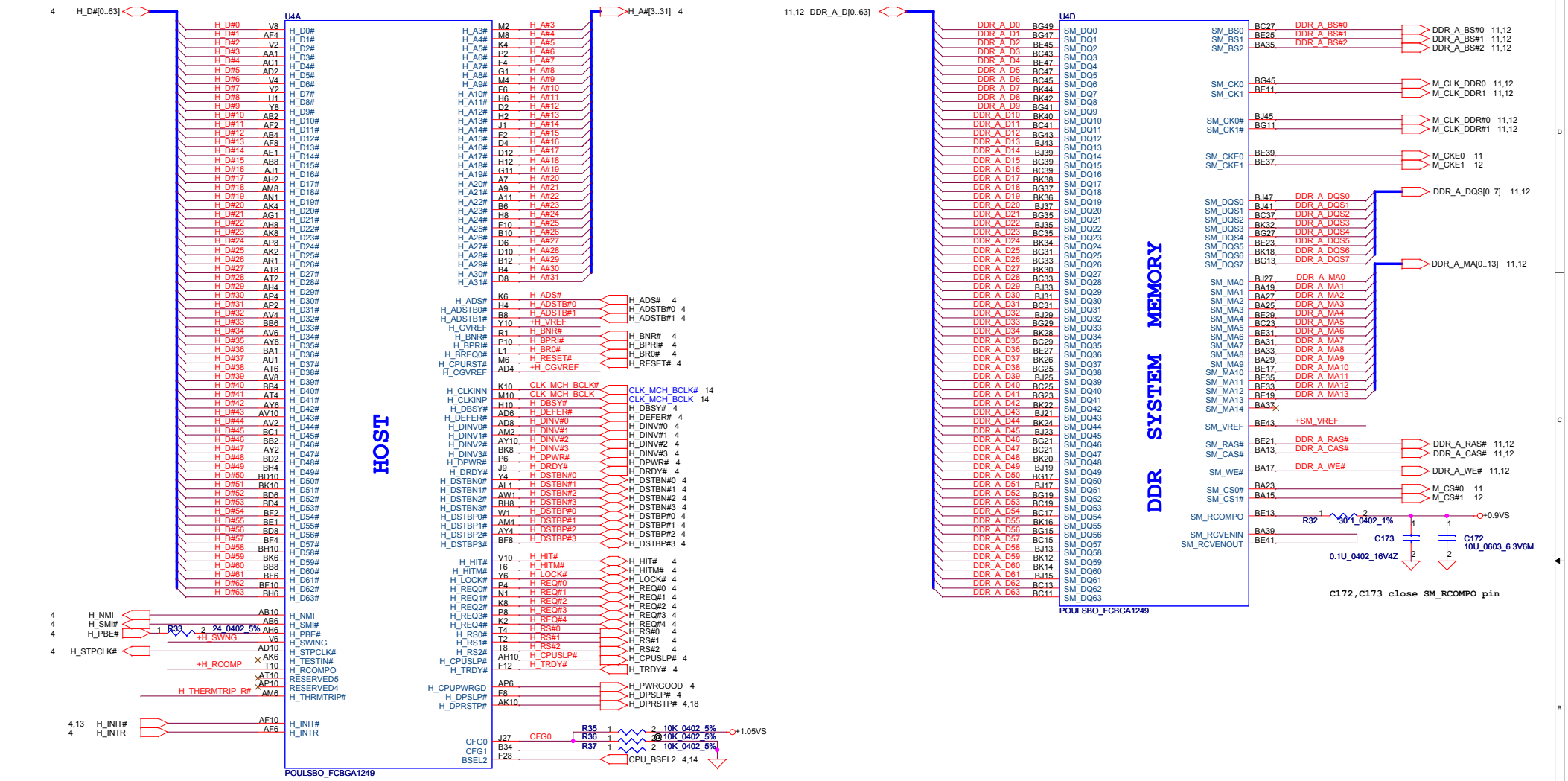
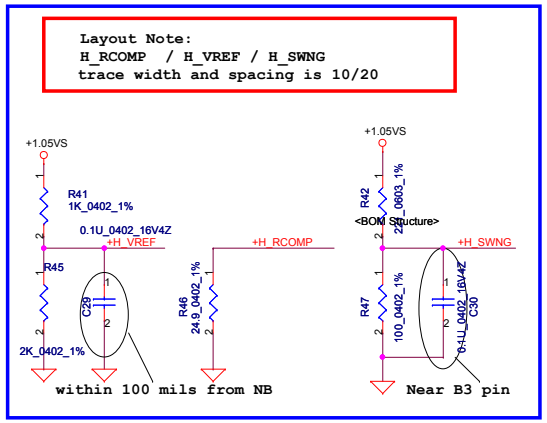
Date: Tuesday, December 02, 2008 | Sheet 5 of 20



layout note:

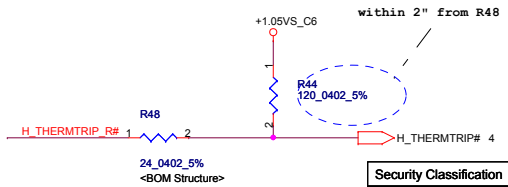
Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces

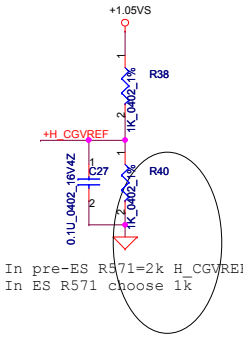


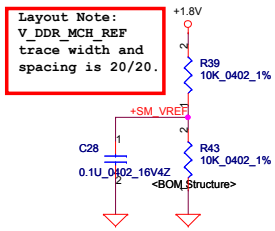
FSB	BSEL2	FSB DDR
100	1	100
133	0	133

FSB	CFG0	FSB DDR
100	1	133
133	0	100

CFG1 10K pull-down is required.







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Title: **Poulsbo(1/5)-HOST/DDR**

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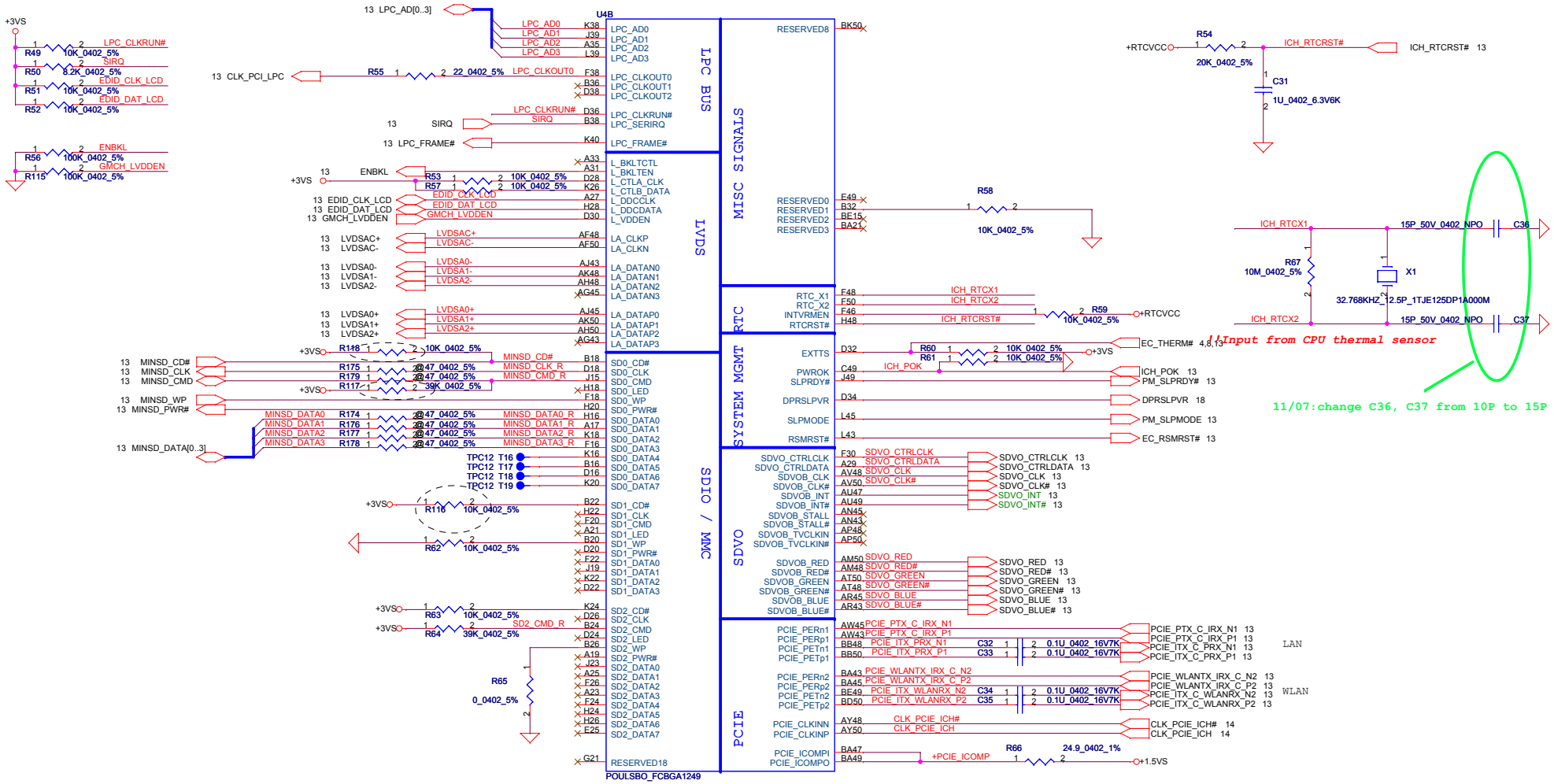
Date: Saturday, December 06, 2008 | Sheet 6 of 20



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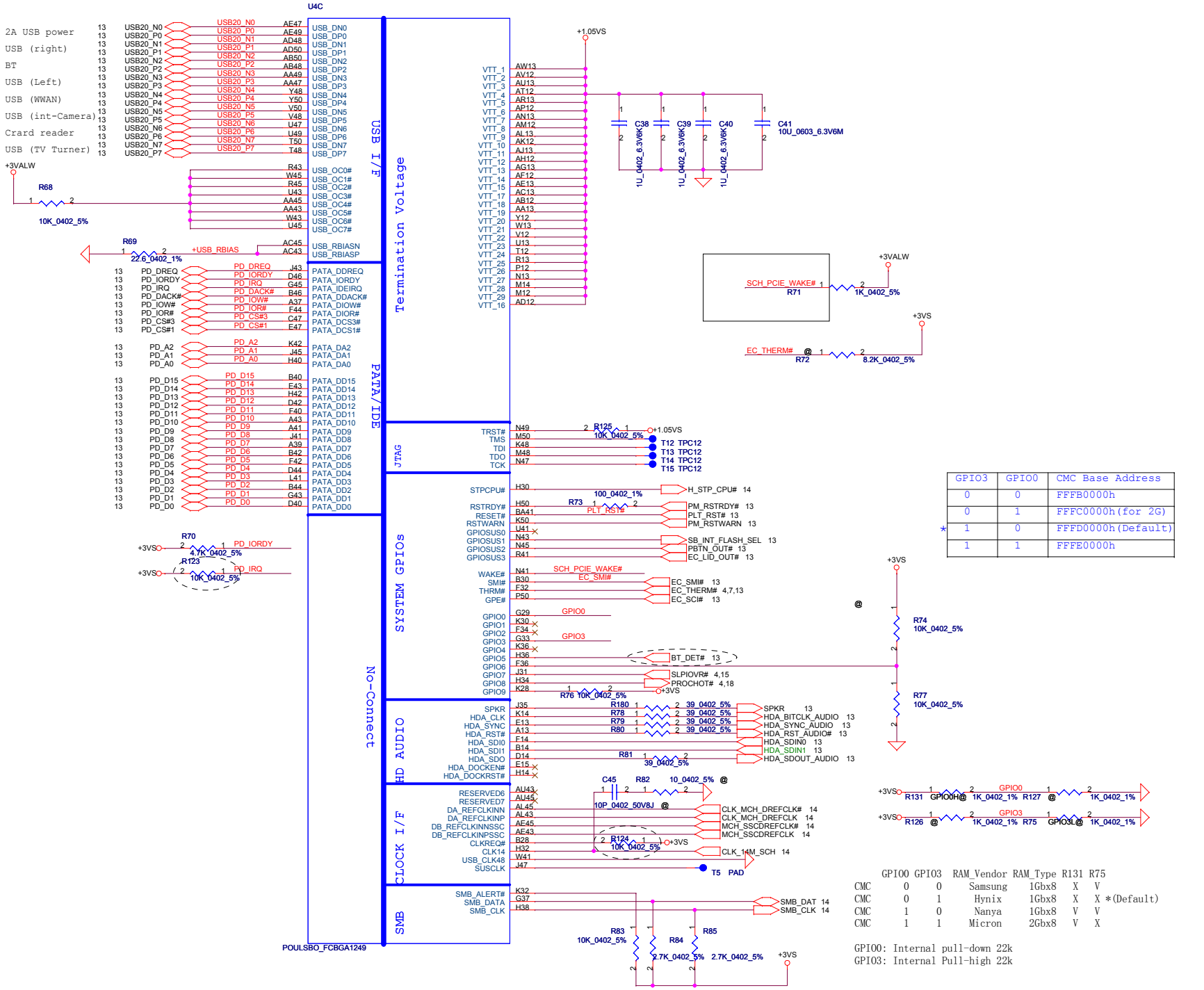
Compal Electronics, Inc.

Title: **Poulsbo(2/5)-LVDS/SDVO/SDIO/PCIE**

Size: Custom | Document Number: KIU10 LS-4764P | Rev: 1.0

Date: Saturday, December 06, 2008 | Sheet 7 of 20



GPIO3	GPIO0	CMC Base Address
0	0	FFFB0000h
0	1	FFFC0000h(for 2G)
* 1	0	FFFD0000h(Default)
1	1	FFFE0000h

	GPIO0	GPIO3	RAM_Vendor	RAM_Type	R131	R75
CMC	0	0	Samsung	1Gbx8	X	V
CMC	0	1	Hynix	1Gbx8	X	X *(Default)
CMC	1	0	Nanya	1Gbx8	V	V
CMC	1	1	Micron	2Gbx8	V	X

GPIO0: Internal pull-down 22k
GPIO3: Internal Pull-high 22k

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Title: Poulsbo(3/5)-HDA/PATA/USB

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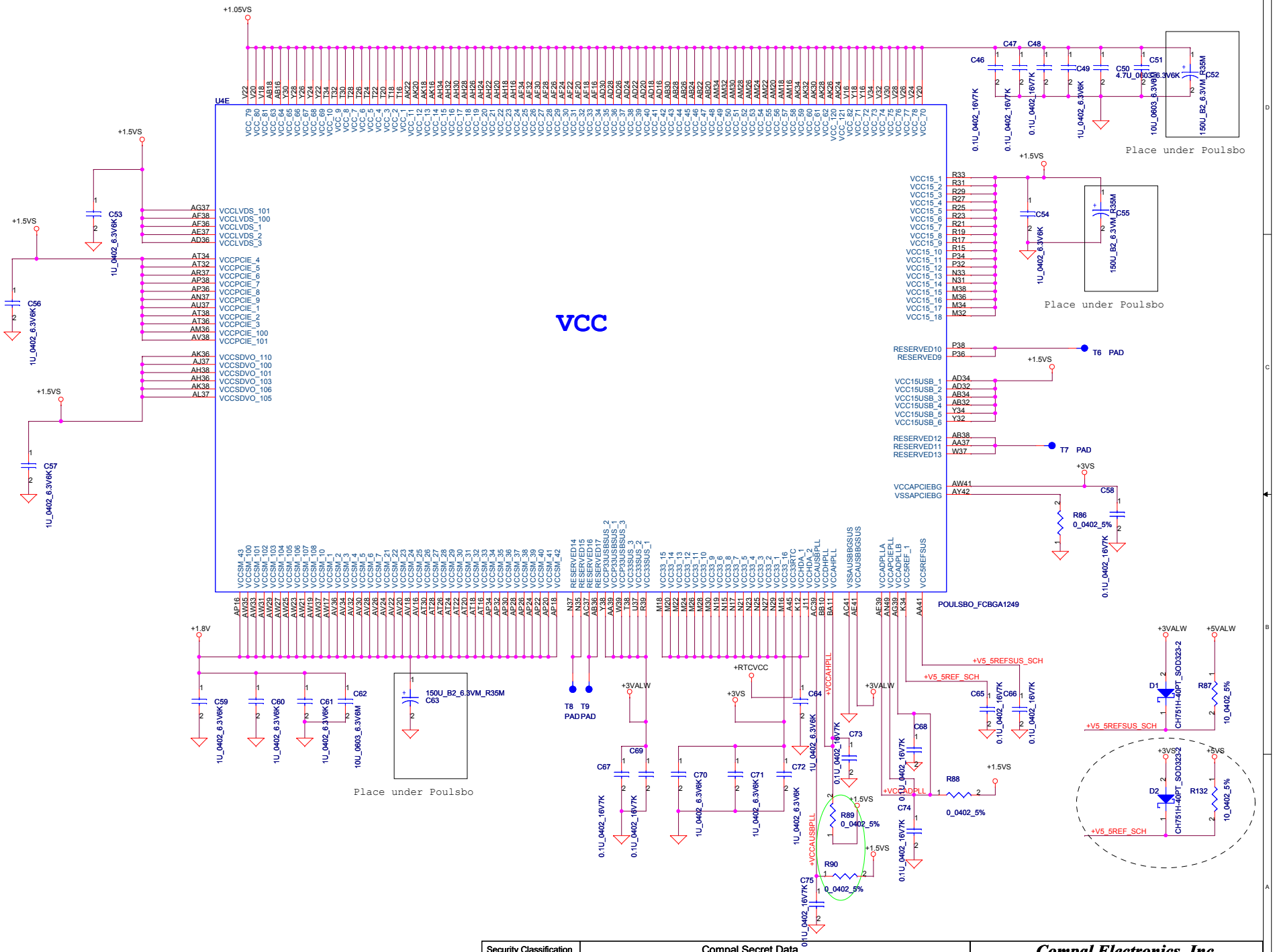
Date: Saturday, December 06, 2008 | Sheet 8 of 20



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Title: **Poulsbo(4/5)-PWR**

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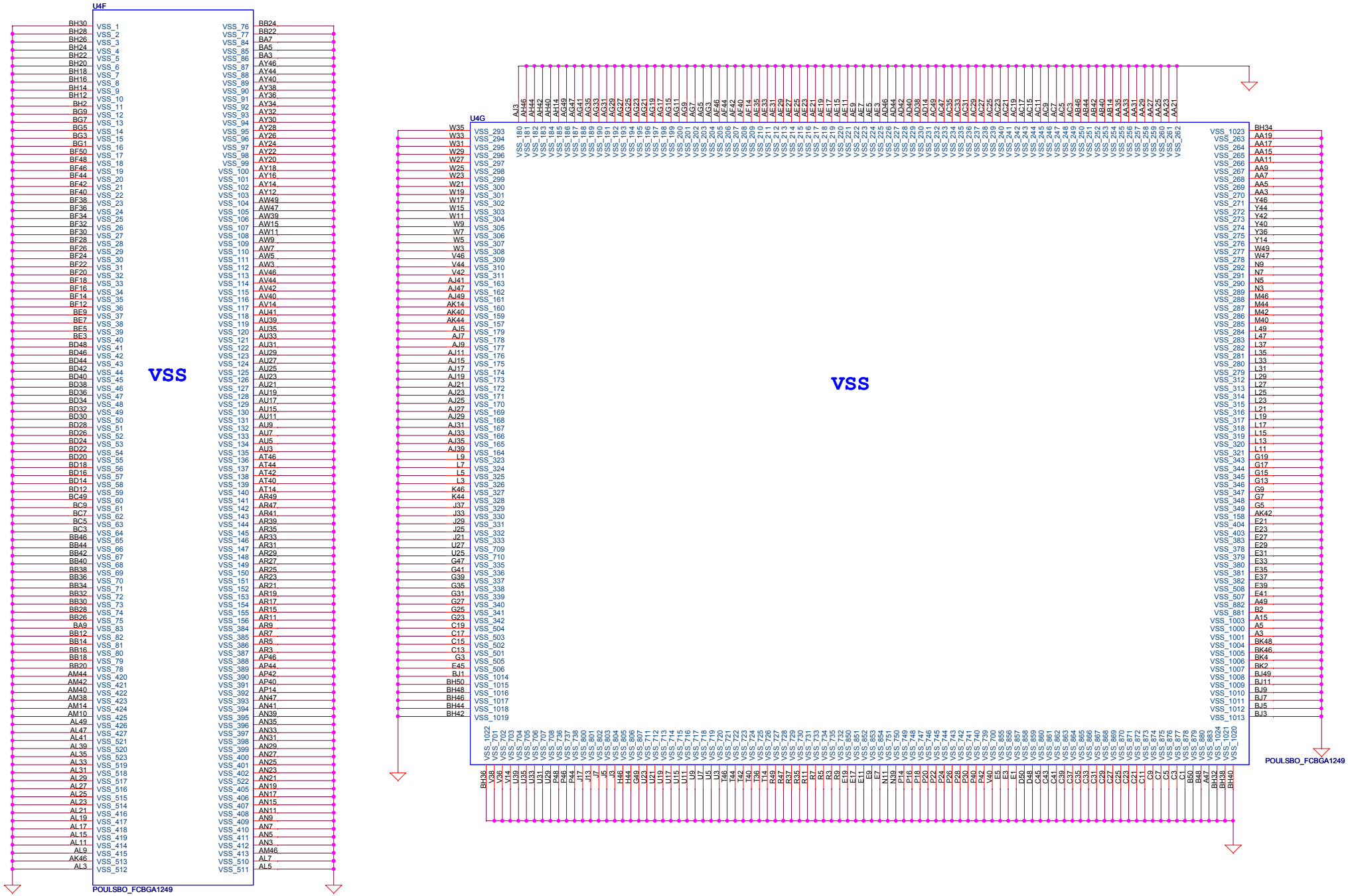

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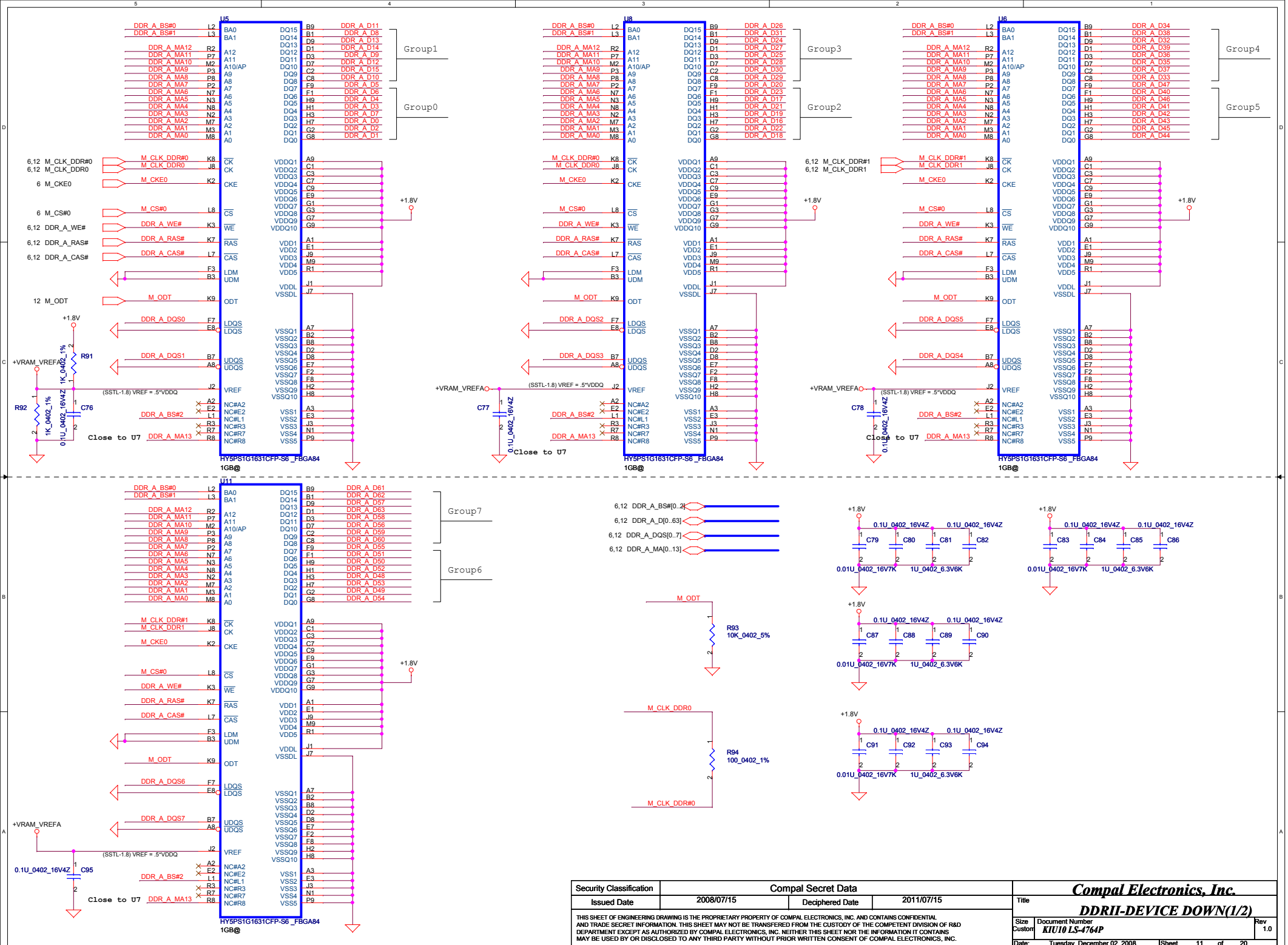
Compal Electronics, Inc.

Title: **Poulsbo(5/5)-GND**

Size: Custom | Document Number: KIU10 LS-4764P | Rev: 1.0

Date: Saturday, December 06, 2008 | Sheet 10 of 20



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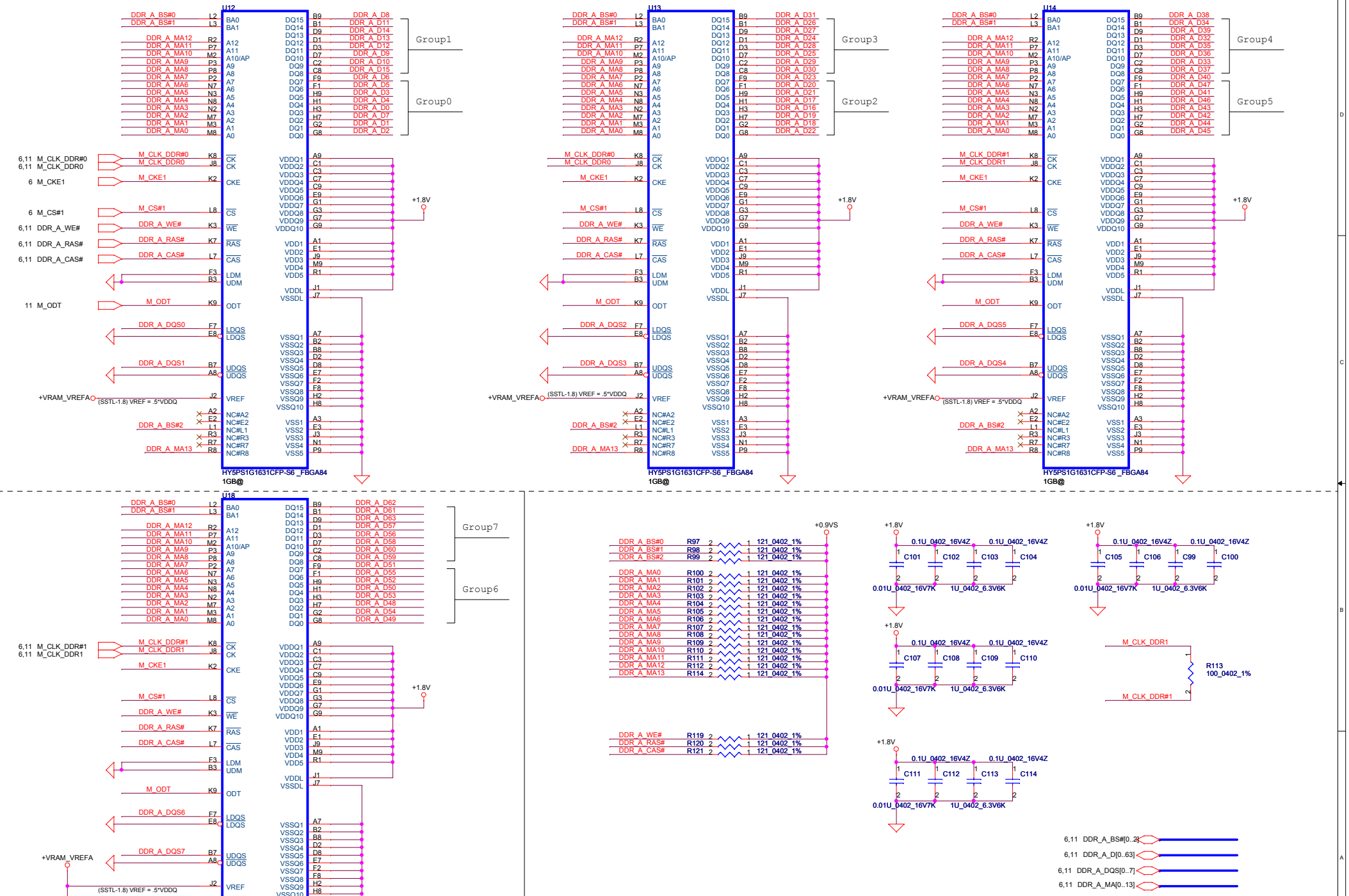
Title: **DDRII-DEVICE DOWN(1/2)**

Size: Custom | Document Number: KIU10 LS-4764P | Rev: 1.0

Date: Tuesday, December 02, 2008 | Sheet 11 of 20



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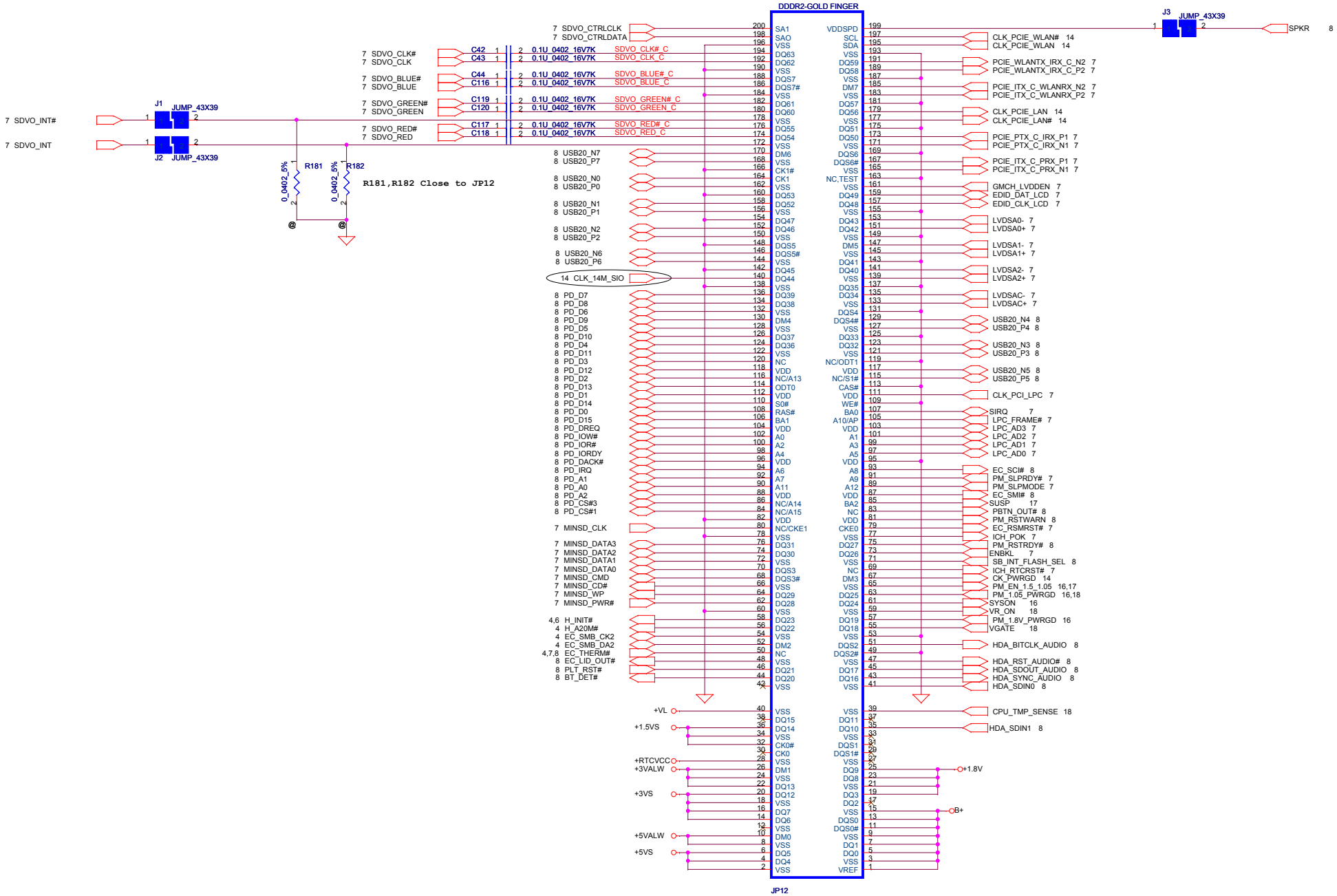
Compal Electronics, Inc.

Title: **DDRII-DEVICE DOWN(2/2)**

Size | Document Number: *KIU10 LS-4764P* | Rev 1.0

Date: Tuesday, December 02, 2008 | Sheet 12 of 20



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Compal Electronics, Inc.

Title: **LVDS/FUN_B/PWR_B/USB_B CONN**

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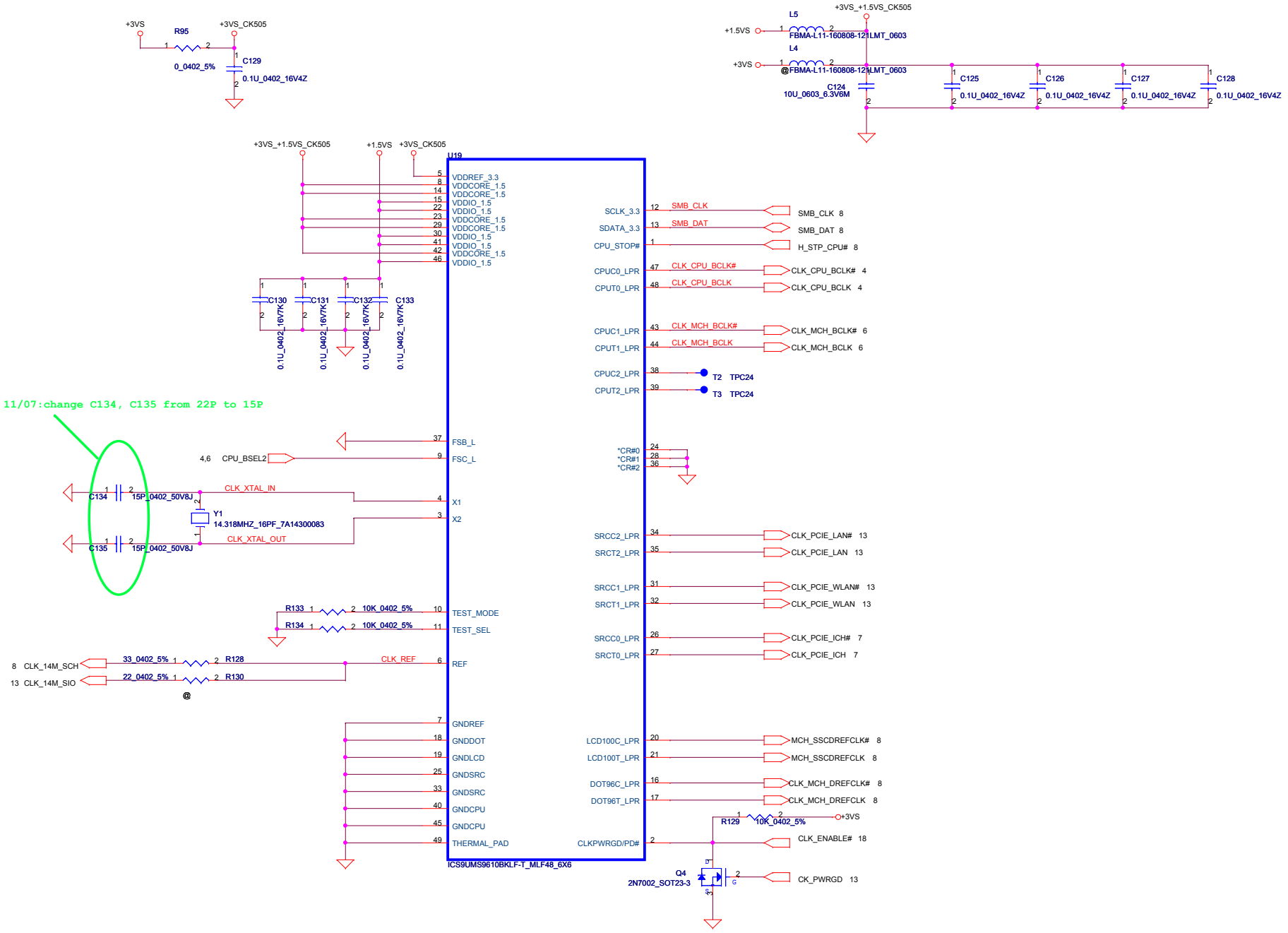
Date: Tuesday, December 02, 2008 | Sheet 13 of 20



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Compal Electronics, Inc.

Title: **Clock Generator CK540**

Size | Document Number: *KIU10 LS-4764P* | Rev 1.0

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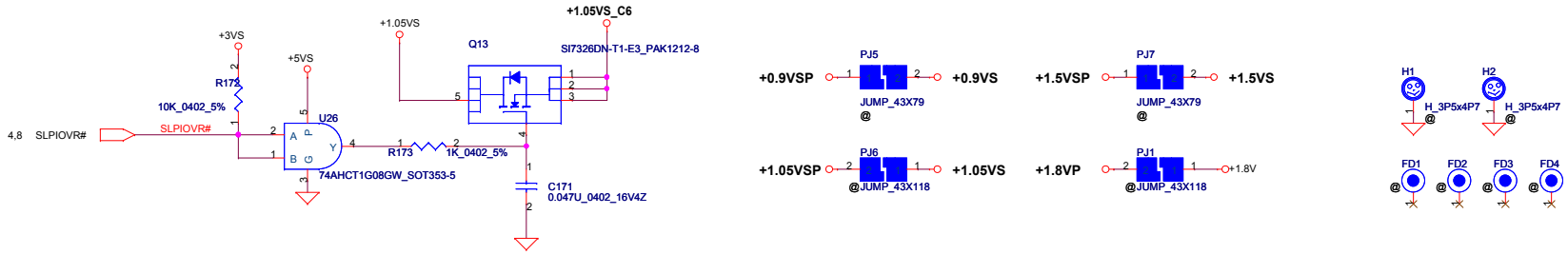

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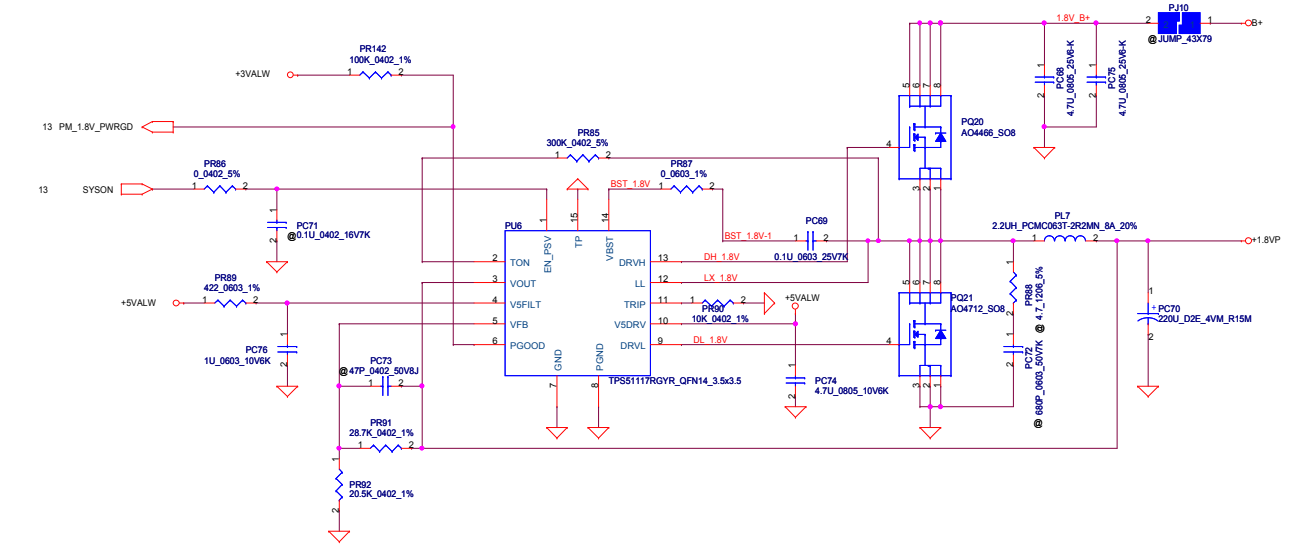
Compal Electronics, Inc.

Title: **DC/DC Circuit**

Size: Custom | Document Number: KIU10 LS-4764P | Rev: 1.0

Date: Tuesday, December 09, 2008 | Sheet 15 of 20



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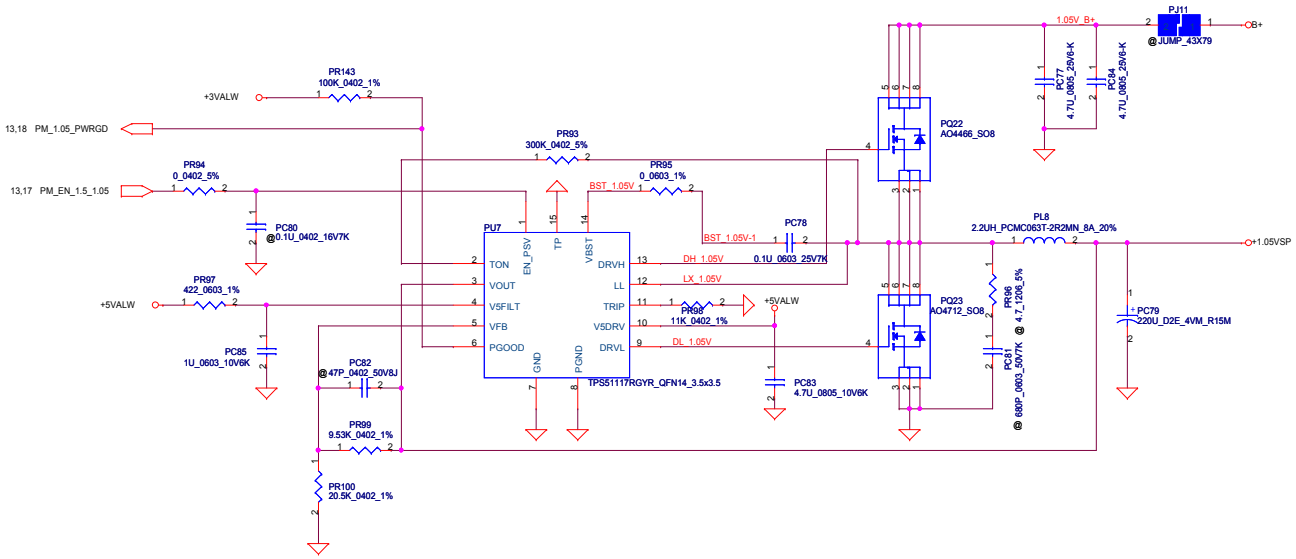

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Issued Date	2008/07/15	Deciphered Date	2011/07/15

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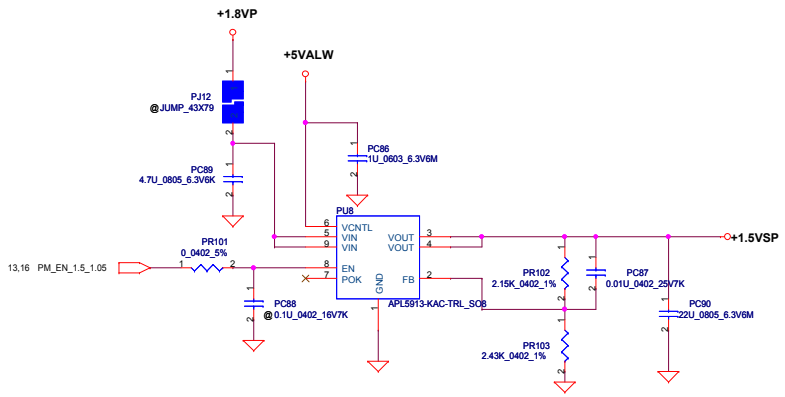
Title: *+1.05VSP / +1.8VP*

Size: C | Document Number: KIU10 LS-4764P | Rev: 1.0

Date: Tuesday, December 02, 2008 | Sheet 16 of 20



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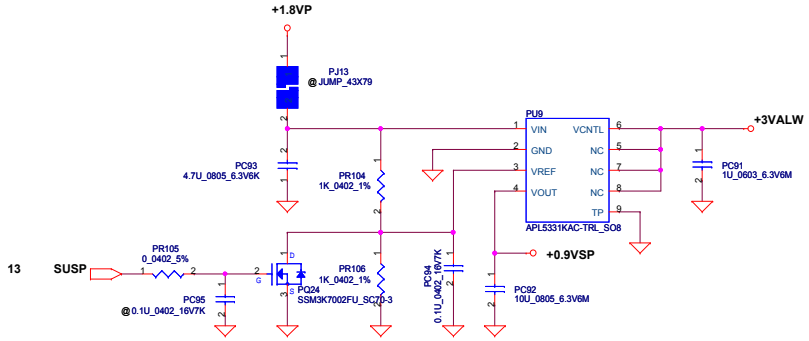

+0.9VSP
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Issued Date	2008/07/15	Deciphered Date	2011/07/15	Title: 1.5V/0.9VSP
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				Date: Tuesday, December 02, 2008; Sheet 17 of 20

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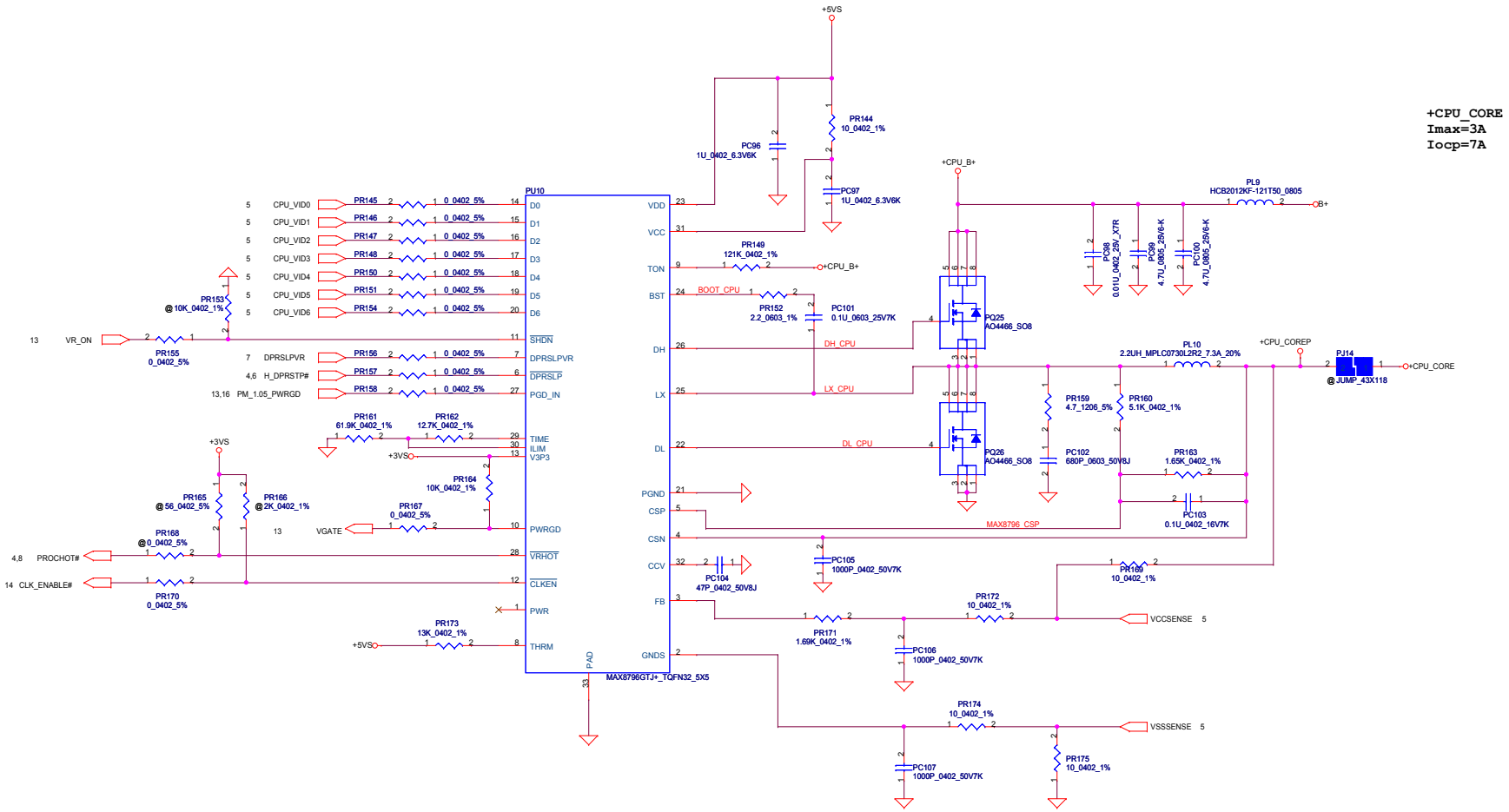

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Issued Date	2008/07/15	Deciphered Date	2011/07/15

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Compal Electronics, Inc.

Title: **CPU_CORE**

Size: C | Document Number: **KIU10 LS-4764P** | Rev: 1.0

Date: Tuesday, December 02, 2008 | Sheet 18 of 20

KIU10 LS-4764P SCHMATIC CHANGE LIST
REVISION CHANGE : 0.1 TO 0.2

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	0907	13	Del J1,J2,J3 Bom structure	Default
2	0907	06	add C172,C173	INTEL Suggestion for avoid ripple noise
3	11/07	07	Change C36, C37 from 10P to 15P	
4	11/07	14	Change C134, C135 from 22P to 15P	

Security Classification	Compal Secret Data		
Issued Date	2008/07/15	Deciphered Date	2011/07/15

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Compal Electronics, Inc.

Title: PIR

Size: Custom | Document Number: KIU10 LS-4764P | Rev: 1.0

Date: Tuesday, December 02, 2008 | Sheet 19 of 20

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
	9/24	16	Change PR99 from 8.2K to 9.53K ohm	3D mark burn-in BSOD issue
	11/10	18	Stuff PR159 and PC102	WWAN noise solution from EMI team requirement
	11/10	18	Change PC98 from 0.01U_0402_25V_X7R	Voltage rating can not meet application

Security Classification	Compal Secret Data		
Issued Date	2005/06/01	Deciphered Date	2006/06/01

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Compal Electronics, Inc.

Title: **Power PIR**

Size | Document Number: *LA-3481P* | Rev: 1.0

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